REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-7, 9-18, 20-32, and 34-41 are pending. Claims 1-7, 9-18, 20-32, and 34-41 stand rejected.

Claims 1, 12, 23, and 26 have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Claim Rejections – 35 U. S. C. § 103

Claims 1-3, 5-7, 9-14, 16-18, 20- 28, 30-32, 34-38, and 40-41 have been rejected under 35 U.S.C. § 103 (a), as being unpatentable over Chehrazi et al., U.S. Patent No. 6,282,556 (hereinafter "Chehrazi") in view of Mennemeier et al., U.S. Patent No. 6,036,350 (hereinafter "Mennemeier").

Applicants have amended claim 1 to include selecting a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector according to a configuration specified by the instruction.

Chehrazi discloses a sum of absolute difference instruction (SABD). In particular, Chehrazi discloses

> FIG. 20A and FIG. 20B illustrate the operation of the sum of absolute differences instruction called the SABD instruction. The SABD instruction of the present invention executes within two execution pipestages and the data is written back in the writeback pipestage. FIG. 20A illustrates an exemplary format 560 of the SABD instruction. <u>The SABD operation computes the differences between corresponding operands stored in the operand registers, Vt and Vs, under control of the format field,</u> determines the absolute value of these differences then adds the absolute value differences together to arrive at a final sum. The resultant sum value is stored in the least significant half word of the destination register, Vd. The operands can be signed or unsigned packed bytes as specified by the formal field 560e. The SABD instruction 560 specifies the source or input registers Vt and Vs by fields 560d and 560c, respectively, and specifies the destination

register, Vd, in field 560b. Different modes of operation are possible of the SABD instruction and these are specified in the mode field 560e.

(Chehrazi, col. 20, lines 42-60) (emphasis added)

Thus, Chehrazi merely discloses computing the difference between corresponding operands stored in the operand registers under control of the format field. In contrast, amended claim 1 refers to selecting a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector according to a configuration specified by the instruction.

Mennemeier, in contrast, discloses sorting signed numbers and solving absolute differences using packed instructions, and similarly to Chehrazi, fails to disclose, teach, or suggest selecting a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector according to a configuration specified by the instruction, as recited in amended claim 1.

Hence, neither Chehrazi, Mennemeier, nor any combination thereof, discloses, teaches, or suggests such limitations of amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Chehrazi in view of Mennemeier.

Given that amended claim 12 contains similar limitations, applicants respectfully submit that amended claim 12 is not obvious under 35 U.S.C. § 103 (a) over Chehrazi in view of Mennemeier.

Because claims 2-3, 5-7, 9-11, 13-14, 16-18, 20-22, and 38 depend from amended claims 1 and 12 respectively, and add additional limitations, applicants respectfully submit that claims 2-3, 5-7, 9-11, 13-14, 16-18, 20-22, and 38 are not obvious under 35 U.S.C. § 103 (a) over Chehrazi in view of Mennemeier.

Applicants have amended claim 23 to include a selector circuit configured to select a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector.

As set forth above, Chehrazi merely discloses computing the difference between corresponding operands stored in the operand registers under control of the format field, and fails to disclose, teach, or suggest a selector circuit configured to select a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector, as recited in amended claim 23.

Mennemeier, in contrast, discloses sorting signed numbers and solving absolute differences using packed instructions, and similarly to Chehrazi, fails to disclose, teach, or suggest a selector circuit configured to select a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector, as recited in amended claim 23.

Hence, neither Chehrazi, Mennemeier, nor any combination thereof, discloses, teaches, or suggests such limitations of amended claim 23.

Therefore, applicants respectfully submit that amended claim 23 is not obvious under 35 U.S.C. § 103 (a) over Chehrazi in view of Mennemeier.

Given that amended claim 26 contains similar limitations, applicants respectfully submit that amended claim 26 is not obvious under 35 U.S.C. § 103 (a) over Chehrazi in view of Mennemeier.

Because claims 24, 27-32, 34-36, 39, 40, and 41 depend from amended claims 23 and 26 respectively, and add additional limitations, applicants respectfully submit that claims 24, 27-32, 34-36, 39, 40, and 41 are not obvious under 35 U.S.C. § 103 (a) over Chehrazi in view of Mennemeier.

Claims 4, 15, 29, and 39 have been rejected under 35 U.S.C. § 103 (a), as being unpatentable over Chehrazi in view of Mennemeier, and further in view of Diefendorff et al., EPO 0485 776A2 (" hereinafter Diefendorff").

Diefendorff, in contrast, discloses graphics pixel packing instructions, and similarly to Chehrazi and Mennemeier, fails to disclose, teach, or suggest selecting a first plurality of numbers from the numbers in the first vector and a second plurality of numbers from the numbers in the second vector according to a configuration specified by the instruction, as recited in amended claim 1.

Because claims 4, 15, 29, and 39 contain similar limitations, applicants respectfully submit that claims 4, 15, 29, and 39 are not obvious under 35 U.S.C. § 103 (a) over Chehrazi in view of Mennemeier, and further in view of Diefendorff.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: 4/12/2007
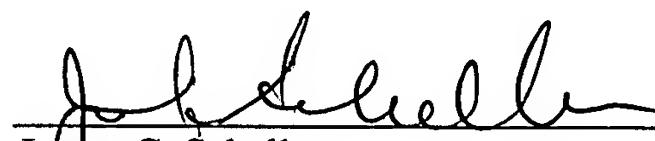
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